AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the below listing of claims that will replace all prior versions and listings of claims in the application. An identifier indicating the status of each claim is provided.

Listing of Claims:

1. (Currently Amended) An operation-processing device for performing operation processing based on an arbitrary operation program, said device comprising:

a register array having a plurality of ~~plural~~ registers each for holding an arbitrary value based on a write address and a write control signal and outputting ~~this~~ the held value to a signal line based on a read address;

an operation portion having an input coupled to said signal line, the operation portion being operable for performing an operation on a value read from said register array to said signal line;

an instruction-decoding portion for decoding an operation instruction from an operation program for operating said operation portion; and

an instruction-execution-controlling portion for controlling said register array and the operation portion in order to execute an operation instruction decoded by said instruction-decoding portion,

wherein said instruction-execution-controlling portion selects one of said registers based on said operation instruction; and

wherein based on a value held by said selected register, said instruction-execution-controlling portion performs register-to-register addressing processing for selecting another of said registers of said register array.

2. (Currently Amended) The operation-processing device according to claim 1, further comprising a read only memory ~~cell~~ in which said operation program is stored.

3. (Currently Amended) The operation-processing device according to claim 1, wherein said operation program includes an operation instruction to perform the register-to-register addressing processing.

4. (Currently Amended) The operation-processing device according to claim ~~1~~ 2,

wherein said register array and the read only memory are each comprised of ~~plural~~ a plurality of memory cells;

wherein said operation portion, the instruction-decoding portion, and the instruction-execution-controlling portion are comprised of ~~plural~~ a plurality of arithmetic/logic operation elements; and

wherein said memory cells and the arithmetic/logic operation elements ~~are constituted of~~ comprise a programmable logic device and are ~~devices~~ formed on ~~the~~ an identical semiconductor chip.

5. (Currently Amended) The operation-processing device according to claim 1, wherein said instruction execution-controlling portion ~~has~~ comprises:

a first selector for selecting any one of a read execution address to select said ~~one~~ selected register and a read address to select ~~this~~ said selected register again; and

a second selector for selecting any one of a write execution address to select said ~~one~~ selected register and a write address to select ~~this~~ said selected register again.

6-13 (Canceled).

14. (Currently Amended) An operation-processing method for performing operation processing based on an arbitrary operation program, said method comprising ~~the steps of~~:

accessing a register array having a plurality of registers, ~~beforehand preparing plural registers~~ each for holding an arbitrary value based on a write address and a write control signal and outputting ~~this~~ the held value to an input of an operation portion based on a read address;

~~thereafter~~ decoding an operation instruction from said operation program;

selecting one of said registers based on said operation instruction;

performing register-to-register addressing processing for selecting, based on a value held by said selected register, another of said registers of said register array ~~register and selecting said another register based on said operation instruction~~; and

performing with said operation portion an operation on a value held by said selected another register ~~and a value of the register selected by said register to register addressing processing~~.

15. (Currently Amended) The operation-processing method according to claim 14, wherein a result of said operation is stored in the register selected on the basis of the value held by said selected another register.

16. (Currently Amended) The operation-processing method according to claim 14, wherein said operation program includes an operation instruction to perform said register-to-register addressing processing.

17-25 (Canceled).

26. (New) The operation-processing device according to claim 1, wherein said input comprises at least one input signal line that is coupled to said signal line via a latch.